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| 09/389,567 | 09/03/1999 | JAY BRUCE ROSS | OGPT-24727 | 5576 |

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| EXAMINER | |
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| ELLIS, RICHARD L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 12 |

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/389,567 | ROSS ET AL. | |
| | Examiner | Art Unit | |
| | Richard Ellis | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *15-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

# REVISED AMENDMENT PRACTICE: 37 CFR 1.121 CHANGED COMPLIANCE IS MANDATORY - Effective Date: July 30, 2003

All amendments filed on or after the effective date noted above must comply with revised 37 CFR 1.121. See Final Rule: **Changes To Implement Electronic Maintenance of Official Patent Application Records** (68 *Fed. Reg.* 38611 (June 30, 2003), posted on the Office's website at: http://www.uspto.gov/web/patents/ifw/ with related information. The amendment practice set forth in revised 37 CFR 1.121, and described below, replaces the voluntary revised amendment format available to applicants since February 2003. **NOTE: STRICT COMPLIANCE WITH THE REVISED 37 CFR 1.121 IS REQUIRED AS OF THE EFFECTIVE DATE (July 30, 2003).** The Office will notify applicants of amendments that are not accepted because they do not comply with revised 37 CFR 1.121 via a Notice of Non-Compliant Amendment. See MPEP 714.03 (Rev. 1, Feb. 2003). The non-compliant section(s) will have to be corrected and the entire corrected section(s) resubmitted within a set period.

***Bold underlined italic font has been used below to highlight the major differences between the revised 37 CFR 1.121 and the voluntary revised amendment format that applicants could use since February, 2003.***
Note: The amendment practice for **reissues** and **reexamination proceedings**, except for drawings, has not changed.

## REVISED AMENDMENT PRACTICE

**I. Begin each section of an amendment document on a separate sheet:**
Each section of an amendment document (*e.g.*, Specification Amendments, Claim Amendments, Drawing Amendments, and Remarks) must begin on a separate sheet. Starting each separate section on a new page will facilitate the process of separately indexing and scanning each section of an amendment document for placement in an image file wrapper.

**II. Two versions of amended part(s) no longer required:**
**37 CFR 1.121 has been revised to no longer require two versions (a clean version and a marked up version) of each replacement paragraph or section, or amended claim. Note, however, the requirements for a clean version and a marked up version for substitute specifications under 37 CFR 1.125 have been retained.**

**A) Amendments to the claims:**
Each amendment document that includes a change to an existing claim, cancellation of a claim or submission of a new claim, **must include a complete listing** of all claims in the application. After each claim number in the listing, the status must be indicated in a parenthetical expression, and **the text of each pending claim** (with markings to show current changes) must be presented. The claims in the listing will replace all prior claims in the application.

(1) The current status of all of the claims in the application, including any previously canceled, not entered or withdrawn claims, must be given in a parenthetical expression following the claim number using only one of the following seven status identifiers: (original), (currently amended), (canceled), (withdrawn), (new), ***(previously presented) and (not entered).*** The text of all pending claims, ***including withdrawn claims,*** must be submitted each time any claim is amended. Canceled ***and not entered*** claims must be indicated by only the claim number and status, without presenting the text of the claims.

(2) The text of all claims being currently amended must be presented in the claim listing with markings to indicate the changes that have been made relative to the immediate prior version. The changes in any amended claim must be shown by underlining (for added matter) or strikethrough (for deleted matter) with 2 exceptions: (1) for ***deletion of five characters or fewer, double brackets may be used (e.g., [[eroor]]); and (2) if strikethrough cannot be easily perceived (e.g., deletion of the number "4" or certain punctuation marks), double brackets must be used (e.g., [[4]]). As an alternative to using double brackets, however, extra portions of text may be included before and after text being deleted, all in strikethrough, followed by including and underlining the extra text with the desired change*** *(e.g., ~~number 4 as~~ number 14 as).* An accompanying clean version is not required and should not be presented. Only claims of the status "currently amended," and "withdrawn" that are being amended, may include markings.

(3) The text of pending claims not being currently amended, ***including withdrawn claims,*** must be presented in the claim listing in clean version, *i.e.*, without any markings. Any claim text presented in clean version will constitute an assertion that it has not been changed relative to the immediate prior version except to omit markings that may have been present in the immediate prior version of the claims.

(4) A claim being canceled must be listed in the claim listing with the status identifier "canceled"; the text of the claim must not be presented. Providing an instruction to cancel is optional.
(5) Any claims added by amendment must be presented in the claim listing with the status identifier "(new)"; the text of the claim must not be underlined.
(6) All of the claims in the claim listing must be presented in ascending numerical order. Consecutive canceled, or not entered, claims may be aggregated into one statement (*e.g.*, Claims 1 – 5 (canceled)).

**Example of listing of claims (use of the word "claim" before the claim number is optional):**

Claims 1-5 (canceled)

Claim 6 (previously presented): A bucket with a handle.

Claim 7 (withdrawn): A handle comprising an elongated wire.

Claim 8 (withdrawn): The handle of claim 7 further comprising a plastic grip.

Claim 9 (currently amended): A bucket with a ~~green~~ blue handle.

Claim 10 (original): The bucket of claim 9 wherein the handle is made of wood.

Claim 11 (canceled)

Claim 12 (not entered)

Claim 13 (new): A bucket with plastic sides and bottom.

**B) Amendments to the specification:**
Amendments to the specification, including the abstract, must be made by presenting a replacement paragraph or section or abstract marked up to show changes made relative to the immediate prior version. An accompanying clean version is not required and should not be presented. Newly added paragraphs or sections, including a new abstract (instead of a replacement abstract), must not be underlined. A replacement or new abstract must be submitted on a separate sheet, 37 CFR 1.72. If a substitute specification is being submitted to incorporate extensive amendments, both a clean version (which will be entered) and a marked up version must be submitted as per 37 CFR 1.125.

The changes in any replacement paragraph or section, or substitute specification must be shown by underlining (for added matter) or strikethrough (for deleted matter) with 2 exceptions: (1) for ***deletion of five characters or fewer, double brackets may be used (e.g., [[eroor]]); and (2) if strikethrough cannot be easily perceived (e.g., deletion of the number "4" or certain punctuation marks), double brackets must be used (e.g., [[4]]). As an alternative to using double brackets, however, extra portions of text may be included before and after text being deleted, all in strikethrough, followed by including and underlining the extra text with the desired change*** *(e.g., ~~number 4 as~~ number 14 as)*

**C) Amendments to drawing figures:**
Drawing changes must be made by presenting replacement figures which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be presented either in the drawing amendments, or remarks, section of the amendment, ***and may be accompanied by a marked-up copy of one or more of the figures being amended, with annotations.*** Any replacement drawing sheet must ***be identified in the top margin as "Replacement Sheet"*** and include all of the figures appearing on the immediate prior version of the sheet, even though only one figure may be amended. ***Any marked-up (annotated) copy showing changes must be labeled "Annotated Marked-up Drawings" and accompany the replacement sheet in the amendment (e.g., as an appendix).*** The figure or figure number of the amended drawing(s) must **not** be labeled as "amended." If the changes to the drawing figure(s) are not accepted by the examiner, applicant will be notified of any required corrective action in the next Office action. No further drawing submission will be required, unless applicant is notified.

Questions regarding the submission of amendments pursuant to the revised practice set forth in this flyer should be directed to: Elizabeth Dougherty or Gena Jones, Legal Advisors, or Joe Narcavage, Senior Special Projects Examiner, Office of Patent Legal Administration, by e-mail to patentpractice@uspto.gov or by phone at (703) 305-1616.

1. Claims 15-34 remain for examination.

2. It is noted that applicant's amendment does not fully comply with the requirements of 37 CFR 1.121 (effective June 30, 2003).

Applicant's amendment fails to comply with the requirements of 37 CFR 1.121 in two areas. First, applicant stated at line 1 of the amendment: "Claims 1-14 have been canceled.". This is incorrect. As clearly shown in the attached flyer detailing the requirements, the only permissible entry for the first line of applicant's amendment is: "Claims 1-14 (Canceled)".

Second, as detailed in section A(2) of the attached flyer, all claims being amended must have markings to indicate the changes made relative to the immediate prior version of that same claim. In the case of claim 23, amended claim 23 states that it is dependent upon claim 16, however, the immediately prior claim 23 was dependent upon claim 22, and no markings have been included to indicate a change of dependency of the claim. New claim 33 also contains the same error, in that new claim 33 is now dependent upon claim 26 instead of claim 32, without any markings to show this change. Further as to claim 23, the word "said" in the phrase "with said set of" with no markings to show deletion of the word "said", and the markings used in claim 23 show deletion of the word "the" from the phrase "with the ... set of", however the word "the" does not appear at that location in the immediately prior claim text.

3. Claims 15 and 13 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3.1. The scope of meaning of the following terms are unclear:

3.1.1. "which said selected is associated with" (claim 15); It appears that applicat omitted the word --opcode-- from between "selected is".

3.1.2. "said input combinations respective single bit results" (claim 23); It appears that applicant omitted several words that should appear between "combinations respective".

4. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

6. This application currently names joint inventors. In considering patentability of the claims under 35 USC § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC § 102(f) or (g) prior art under 35 USC § 103.

7. Claims 15, 17-20 22, 25, 27-30, and 32 are rejected under 35 USC § 102(b) as being clearly anticipated by Hastings et al., *When is a Memory not a Memory*, Electro/87 and Mini/Micro Northeast Conference Record, Electronic Conventions Management, 1987.

Hastings et al. taught the invention as claimed (as per claim 15), including a data processing ("DP") system comprising:

7.1. a bit stream processor (fig. 1);

7.2. a memory (1Kx8 MEMORY) having one or more inputs for receiving respective input bit streams (A, B), said input bit streams of said one or more inputs defining a sequence of input combinations to said memory (inherent);

7.3. an opcode input (OP) of said memory for inputting a selected opcode, which said selected [opcode] is associated with a function (OP = 00 Addition, 01 Subtraction, 10 Multiplication, 11 Division) wherein said associated function (Addition, Subtraction, Multiplication, Division) operates on said sequence of input combinations (A, B) to generate an output bit stream (C1, C0); and,

7.4. an output of said memory (C1, C0) for outputting an output bit stream.

8. As to claim 17, Hastings et al. taught that the memory comprised binary memory devices which can be individually and selectively read (by stating that the device was a memory, Hastings et al. has inherently stated this claim).

9. As to claim 18, Hastings et al. taught that the sequence of input combinations comprise separate address inputs which are selected by said associated function (pg. 2, col. 1).

10. As to claim 19, Hastings et al. taught that the associated function was a function of one or more Boolean operations (boolean Addition, boolean Subtraction, boolean Multiplication, boolean Division).

11. As to claim 20, Hastings et al. taught that each said input combination of said sequence of input combinations at said one or more inputs was operated on by said associated function (pg. 2, cols. 1 and 2).

12. As to claim 22, Hastings et al. taught that the opcode is associated with a function defined by a predetermined set of Boolean operations (fig. 1, OP = 00 = Addition, etc.).

13. As to claims 25, 27-30, and 32, they do not teach or define above the invention claimed in claims 15-24 and are therefore rejected under Hastings et al. for the same reasons set fourth in the rejection of claims 15-24, supra.

14. Claims 16, 21, 23, 24, 26, 31, and 33-34 are rejected under 35 USC § 103 as being unpatentable over Hastings et al., in view of Ohta et al., *New FPGA Architecture for Bit-Serial Pipeline Datapath*, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, April 15-17, 1998.

Ohta et al. was cited as a prior art reference in paper number 6, mailed May 1, 2003.

15. As to claim 16, Hastings et al. taught that the memory was a bit-addressable memory (pg. 1, col. 1, first paragraph) where each said input combination of said sequence of input combinations is mapped to a single bit location in said memory (applicant has claimed here the definition of a memory).

16. As to claim 21, Hastings et al. taught that the one or more inputs accommodates a single seal bit stream (A, B).

17. As to claim 23, Hastings et al. taught that said function is represented by a lookup table (1kx8 MEMORY) mapping a finite number of said input combinations [to] respective single bit results (pg. 2, col. 1, first paragraph) said respective single bit results obtained by applying a set of predetermined Boolean operations to said input combinations (Addition, Subtraction,

Multiplication, Division).

18. As to claim 24, Hastings et al. taught that each said respective single bit results of said finite number of said input combinations was used to generate a string of said single bit results which define said associated function (pg. 2, col. 1, third full paragraph, pg. 2, col. 2, first through third paragraphs).

19. As to claims 26, 31, and 33-34, they do not teach or define above the invention claimed in claims 16, 21, and 23-24 and are therefore rejected under Hastings et al. in view of Ohta et al. for the same reasons set fourth in the rejection of claims 16, 21, and 23-24 , supra.

20. As to claims 16, 21, 23, 24, 26, 31, and 33-34, Hastings et al. did not specifically teach that the information was single bit and/or bit serial. However, Ohta et al. taught a system design for producing computational elements that were single bit computational elements (section 2, first paragraph). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have modified Hastings et al. to accept and produce single bit results because of Ohta et al.'s teaching that designing computational elements as single bit elements produces significant time/space and speed advantages (section 2, first through fourth paragraphs).

21. Claims 15, 17-20 22, 25, 27-30, and 32 are rejected under 35 USC § 102(b) as being clearly anticipated by Bradley et al., U.S. Patent 4,608,659.

Bradley et al. taught the invention as claimed (as per claim 15), including a data processing ("DP") system comprising:

21.1. a bit stream processor (fig. 1);

21.2. a memory (fig. 4, 84) having one or more inputs for receiving respective input bit streams (APORT, BPORT), said input bit streams of said one or more inputs defining a sequence of input combinations to said memory (because the memory 84 is used as the adder/subtracter in Bradley et al.'s system, it will inherently receive a sequence of input combinations);

21.3. an opcode input (ADD/SUB) of said memory for inputting a selected opcode, which

said selected [opcode] is associated with a function (addition, subtraction) wherein said associated function (addition, subtraction( operates on said sequence of input combinations (APORT, BPORT) to generate an output bit stream (E); and,

21.4. an output of said memory (E) for outputting an output bit stream.

22. As to claim 17, Bradley et al. taught that the memory comprised binary memory devices which can be individually and selectively read (by teaching that the memory 84 was a memory, Bradley et al. has inherently taught that it comprised binary memory devices that can be individually and selectively read, because this is the very definition of a memory. Additionally, Bradley et al. taught the exact binary memory values that are readable as table 3 starting at col. 22).

23. As to claim 18, Bradley et al. taught that the sequence of input combinations comprise separate address inputs which are selected by said associated function (col. 20 line 65 to col. 21 line 9).

24. As to claim 19, Bradley et al. taught that the associated function was a function of one or more Boolean operations (addition/subtraction).

25. As to claim 20, Bradley et al. taught that each said input combination of said sequence of input combinations at said one or more inputs was operated on by said associated function (col. 21 lines 11-17).

26. As to claim 22, Bradley et al. taught that the opcode is associated with a function defined by a predetermined set of Boolean operations (col. 21 lines 11-17).

27. As to claims 25, 27-30, and 32, they do not teach or define above the invention claimed in claims 15-24 and are therefore rejected under Bradley et al. for the same reasons set fourth in the rejection of claims 15-24, supra.

28. Claims 16, 21, 23, 24, 26, 31, and 33-34 are rejected under 35 USC § 103 as being unpatentable over Bradley et al., in view of Ohta et al., *New FPGA Architecutre for Bit-Serial Pipeline Datapath*, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, April 15-17, 1998.

Ohta et al. was cited as a prior art reference in paper number 6, mailed May 1, 2003.

29. As to claim 16, Bradley et al. taught that the memory was a bit-addressable memory (84) where each said input combination of said sequence of input combinations is mapped to a single bit location in said memory (Table 3, col. 22, et seq.).

30. As to claim 21, Bradley et al. taught that the one or more inputs accomidates a single seal bit stream (APORT, BPORT).

31. As to claim 23, Bradley et al. taught that said function is represented by a lookup table (Table 3, col. 22) mapping a finite number of said input combinations [to] respective single bit results (Table 3, OP1, OP2, RESULT) said respective single bit results obtained by applying a set of predetermined Boolean operations to said input combinations (addition/subtraction).

32. As to claim 24, Bradley et al. taught that each said respective single bit results of said finite number of said input combinations was used to generate a string of said single bit results which define said associated function (Table 3).

33. As to claims 26, 31, and 33-34, they do not teach or define above the invention claimed in claims 16, 21, and 23-24 and are therefore rejected under Bradley et al. in view of Ohta et al. for the same reasons set fourth in the rejection of claims 16, 21, and 23-24, supra.

34. As to claims 16, 21, 23, 24, 26, 31, and 33-34, Bradley et al. did not specifically teach that the information was single bit and/or bit serial. However, Ohta et al. taught a system design for producing computational elements that were single bit computational elements section 2, first paragraph). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have modified Bradley et al. to accept and produce single bit results because of Ohta et al.'s teaching that designing computational elements as single bit elements produces significant time/space and speed advantages section 2, first through fourth paragraphs).

35. Claims 15-34 are rejected under 35 USC § 102(b) as being clearly anticipated by Stratton, III, U.S. Patent 4,608,659.

Stratton, III taught the invention as claimed as per claim 15), including a data processing "DP") system comprising:

35.1. a bit stream processor (fig. 2);

35.2. a memory (13a) having one or more inputs for receiving respective input bit streams (1, 2, 4, 8, 16, 32), said input bit streams of said one or more inputs defining a sequence of input combinations to said memory (col. 1 lines 16-36);

35.3. an opcode input (64, 128) of said memory (13a) for inputting a selected opcode, which said selected [opcode] is associated with a function (character conversion) wherein said associated function (character conversion) operates on said sequence of input combinations (1, 2, 4, 8, 16, 32) to generate an output bit stream (lines from memory 13a to CPU 14); and,

35.4. an output of said memory (lines from memory 13a to CPU 14) for outputting an output bit stream.

36. As to claim 16, Stratton, III taught that the memory was a bit-addressable memory (fig. 3, 32a, 32b) where each said input combination of said sequence of input combinations is mapped to a single bit location in said memory (col. 4 lines 3-15).

37. As to claim 17, Stratton, III taught that the memory comprised binary memory devices which can be individually and selectively read (by teaching that the memory 13a was a ROM, Stratton, III has inherently taught that it comprised binary memory devices that can be individually and selectively read because applicat has merely claimed the very definition of a memory in this claim. Additionally see fig. 3 where Stratton, III details that the internals of the ROM's contain "bit" memories (32a, 32b)).

38. As to claim 18, Stratton, III taught that the sequence of input combinations comprise separate address inputs which are selected by said associated function (col. 1 line 66 to col. 2 line 1).

39. As to claim 19, Stratton, III taught that the associated function was a function of one or more Boolean operations (character code conversion).

40. As to claim 20, Stratton, III taught that each said input combination of said sequence of input combinations at said one or more inputs was operated on by said associated function (character code conversion).

41. As to claim 21, Stratton, III taught that the one or more inputs accomidates a single seal bit stream (fig. 3, 1024 bit memory).

42. As to claim 22, Stratton, III taught that the opcode is associated with a function defined by a predetermined set of Boolean operations (fig. 2, BCD to 6000, ASCII to 6000).

43. As to claim 23, Stratton, III taught that said function is represented by a lookup table (32a, 32b, col. 3 lines 57-67) mapping a finite number of said input combinations [to] respective single bit results (col. 1 line 66 to col. 2 line 1) said respective single bit results obtained by applying a set of predetermined Boolean operations to said input combinations (character conversion).

44. As to claim 24, Stratton, III taught that each said respective single bit results of said finite number of said input combinations was used to generate a string of said single bit results which define said associated function (col. 1 lines 16-36).

45. As to claims 25-34, they do not teach or define above the invention claimed in claims 15-24 and are therefore rejected under Stratton, III for the same reasons set fourth in the rejection of claims 15-24, supra.

46. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

47. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

RICHARD L. ELLIS
PRIMARY EXAMINER

Richard Ellis
April 20, 2004